REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the non-final Office Action of February 10, 2005 (hereinafter "Office Action"). In response, Applicants submit that the cited references fail to disclose or suggest, at least, all of the recitations of the pending independent claims; therefore, Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Independent Claims 1 and 11 are Patentable

Independent Claims 1 and 11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent No. 5,450,365 to Adachi (hereinafter "Adachi") in view of Japanese Patent No. JP404271673 to Kaneko (hereinafter "Kaneko"). Independent Claim 1 is directed to a memory interface system and recites:

> at least one channel line that couples a memory to a memory controller, the at least one channel line being responsive to a terminal voltage that is independent of a memory supply voltage and a memory controller supply voltage.

Independent Claim 11 includes similar recitations. As illustrated in FIG. 1, for example, of the present Specification, a memory interface system is shown in which the terminal voltage VTER is independent of the memory supply voltage VDD1 and the memory controller supply voltage VDD2. The Office Action alleges that Adachi discloses a memory card 14 that is responsive to an independent memory supply voltage, a memory controller 10 that is responsive to an independent 5V supply voltage, and channel lines 122 and 124 that are responsive to the 3V supply voltage, which is independent of the 5V supply voltage and the memory card 14 supply voltage. (Office Action, pages 3 and 4).

Applicants respectfully disagree with this interpretation of the teachings of Adachi. In particular, Applicants refer to column 3 of Adachi where it is explained that the logic circuit 22 comprises part of the memory controller. Adachi describes the logic circuit 22 as follows:

> Specifically, the logic circuit 22 generates a control signal matching the kind of the memory card 14 connected to the connector 12, thereby controlling the write-in and read-out of data. (Adachi, col. 3, lines 37 - 40)

As shown in the Figure of Adachi, the logic circuit 22 is responsive to the same 3V power supply that is used to power the I/O lines 122 and 124. Thus, in sharp contrast to the recitations of Claims 1 and 11, the I/O lines 122 and 124 are not responsive to a terminal voltage that is independent of a memory controller supply voltage as the logic circuit 22, which comprises part of the memory controller, is responsive to the same 3V power supply used to power the I/O lines 122 and 124.

Accordingly, for at least the foregoing reasons, Applicants respectfully submits that independent Claims 1 and 11 are patentable over Suh in view of Merritt and Taguchi and that Claims 2 – 10 and 12 - 20 are patentable at least per the patentability of independent Claims 1 and 11.

Independent Claims 1 and 11 also stand rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent No. 6,078,978 to Suh (hereinafter "Suh") in view of U. S. Patent No. 6,185,145 to Merritt (hereinafter "Merritt") and U. S. Patent No. 6,184,737 to Taguchi (hereinafter "Taguchi"). The Office Action alleges that when the teachings of the Suh, Merritt, and Taguchi references are combined, independent Claims 1 and 11 are rendered obvious. (Office Action, 7).

Applicants respectfully disagree with this interpretation of the teachings of Suh, Merritt and Taguchi. Turning first to Suh, Applicants acknowledge that Suh describes a bus interface circuit shown in FIG. 1 in which a reference voltage Vref is generated based on a terminal voltage Vtt using an off-chip network of resistors R1 and R2 (Suh, col. 2, lines 1 – 20). Applicants submit, however, that Suh appears to be silent with regard to the voltage source used to power the receiver 13. Suh explains that the "environment of the transmission line for the data signal is different than that of the transmission line for the reference voltage signal." (Suh, col. 4, lines 32 – 34). Thus, while Suh describes interface circuits in which the transmission line for the reference voltage signal is off-chip while a transmission line for a data signal is on-chip, Suh does not appear to describe what voltage is used to power the receiver 13. Thus, Suh contains no teaching or suggestion of making the voltage that drives the receiver 13 and the terminal voltage Vtt independent from one another.

Turning next to Merritt, this reference discloses a system in FIG. 1 in which the voltage VCC2 used to power the logic section 200 is also used to drive the line carrying the data signal VIN. Thus, Merritt does not disclose a system in which the voltage used to drive the data line is independent of the logic section 200.

Turning finally to Taguchi, this reference discloses a bus transmission system in FIGS. 7 and 9 in which the transmission lines 10 and 11 are responsive to the voltage Vtt and the device 30 is also responsive to the same voltage Vtt as shown, for example, in FIG. 9 where the transmission lines 10 and 11 are responsive to the Vtt power supply voltage of 2.5 volts and the input and output buffers 32 and 33 are powered by the same Vtt power supply voltage of 2.5 volts. Thus, the voltage used to drive the transmission lines 10 and 11 is not independent of the voltage used to drive the device 30.

In view of the analysis above, Applicants respectfully submit that Suh, Merritt, and Taguchi, either alone or in combination, do not disclose or suggest a channel line that is responsive to a terminal voltage that is independent of a memory supply voltage and a memory controller supply voltage as recited in Claims 1 and 11.

Accordingly, for at least the foregoing reasons, Applicants respectfully submits that independent Claims 1 and 11 are patentable over Suh in view of Merritt and Taguchi and that Claims 2 – 10 and 12 - 20 are patentable at least per the patentability of independent Claims 1 and 11.

Dependent Claims 10 and 20 are Separately Patentable

Applicants respectfully submit that dependent Claims 10 and 20 are patentable over the cited references for at least the reasons set forth above with respect to Claims 1 and 11. Dependent Claims 10 and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Suh in view of Merritt and Taguchi. Dependent Claims 10 and 20 also stand rejected under 35 U.S.C. §103(a) as being unpatentable over Adachi in view of Kaneko and Taguchi.

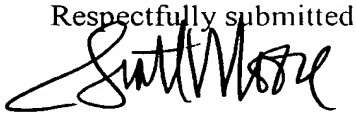
Claims 10 and 20 recite that the magnitude of the terminal voltage is greater than the magnitudes of the memory supply voltage and the controller supply voltage, respectively. Applicants submit that none of the cited references disclose or suggest using a terminal voltage that has a magnitude greater than the magnitudes of the memory supply voltage and the controller supply voltage, respectively, as recited in Claims 10 and 20.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that dependent Claims 10 and 20 are separately patentable over Suh, Merritt, Kaneko, and Taguchi.

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,



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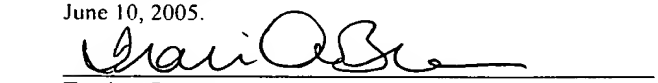

Traci A. Brown